



Patent Application
Attorney Docket No.: 57941.000063
Client Reference No.: RA001.2003.2.C.US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: :
:
Michael FARMWALD et al. :
: Group Art Unit: Unassigned
Appln. No.: 10/716,596 :
: Examiner: Unassigned
Filed: November 20, 2003 :
:
For: INTEGRATED CIRCUIT I/O USING :
A HIGH PERFORMANCE BUS :
INTERFACE :

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with the duty under 37 C.F.R. § 1.56 of each individual associated with the filing and prosecution of the above-identified patent application (hereinafter, "associated individuals") to disclose all information known to that individual to be material to patentability, Applicant(s) hereby submits attached Form PTO-1449 (modified) listing cited references. This submission is made in accordance with 37 C.F.R. §§ 1.97 and 1.98 and § 609 of the Manual of Patent Examining Procedure.

The cited references, while believed to be of some relevance, are not necessarily considered to teach or suggest any aspect of the invention described and claimed in the above-

identified patent application. Applicant(s) hereby expressly reserves the right to swear behind the effective dates of any of the cited references. Applicant(s) further reserves the right to question the relevance, materiality, and/or prior art status of any of the cited references in whole, in part, or in combination, subsequent to the filing of this information disclosure statement. This information disclosure statement is also not to be construed as a representation that a search has, or has not, been conducted or that no better art exists. Rather, this information disclosure statement discloses only the best references of which the associated individuals are aware.

The Examiner is respectfully requested to consider each of the cited references, to indicate such consideration by initialing in the space provided next to each cited reference on the enclosed Form PTO-1449 (modified), to sign the initialed Form PTO-1449 (modified), and to return a copy of the same with the next communication to the Applicant(s).

Since copies of the cited references were previously submitted in prior U.S. Patent Application No. 10/037,171, copies of the cited references are not being submitted herewith. However, copies will be forwarded at the request of the Examiner.

In accordance with 37 CFR § 1.97(b), this information disclosure statement is being filed (i) within three months of the filing date of the above-identified patent application; (ii) within three months of the date upon which the above-identified patent application entered the national stage as set forth in 37 CFR § 1.491; or (iii) before the mailing date of a first Office Action on the merit for the above-identified patent application. Accordingly, no statement or fee is required.

Please charge any shortage in fees due in connection with the filing of this communication to Deposit Account No. 50-0206, and please credit any excess fees to such deposit account.

Respectfully submitted,

Hunton & Williams LLP

By: 

Thomas E. Anderson
Registration No. 37,063

TEA/sdw

Hunton & Williams LLP
1900 K Street, N.W.
Washington, D.C. 20006-1109
Telephone: (202) 955-1500
Facsimile: (202) 778-2201

Date: February 6, 2004

FEB 06 2004

1 of 19

| | | |
|--|---|------------------------------|
| PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT | ATTY. DOCKET NO. 57941.000063 | SERIAL NUMBER 10/716,596 |
| | APPLICANT(S) MICHAEL FARMWALD ET AL. | |
| | FILING DATE November 20, 2003 | GROUP ART UNIT Unassigned |

U.S. PATENT DOCUMENTS

| <u>EXAMINER INITIALS</u> | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|------------------------------|----|--------------------|---------------|-------------|-------|--------------|----------------|
| | 1. | 5,034,964 | Jul. 23, 1991 | Khan et al. | | | |
| | 2. | 4,755,937 | July 5, 1989 | Glier | | | |
| | 3. | 4,875,192 | Oct 17, 1989 | Matsumoto | | | |

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

| | | |
|--|-----|--|
| | 4. | Hansen et al., "A RISC MICROPROCESSOR WITH INTEGRAL MMU AND CACHE INTERFACE", MIPS Computer Systems, Sunnyvale, CA, IEEE 1986 pp 145-148 |
| | 5. | Moussouris et al., "A CMOS PROCESSOR WITH INTEGRATED SYSTEMS FUNCTIONS", MIPS Computer Systems, Sunnyvale, CA, IEEE 1986 pp 126-130 |
| | 6. | "LR2000 High Performance RISC Microprocessor Preliminary" LSI Logic Corp. 1988, pp. 1-15 |
| | 7. | "LR2010 Floating Point Accelerator Preliminary" LSI Logic Corp. 1988, pp 1-20 |
| | 8. | "High Speed CMOS Databook", Integrated Device Technology Inc. Santa Clara, CA, 1988 pp 9-1 to 9-14 |
| | 9. | Riordan T. "MIPS R2000 Processor Interface 78-00005(C)", MIPS Computer Systems, Sunnyvale, CA, June 30, 1987, pp 1-83 |
| | 10. | Moussouris, J. "The Advanced Systems Outlook-Life Beyond RISC: The next 30 years in high-performance computing", Computer Letter, July 31, 1989 (an edited excerpt from an address at the fourth annual conference on the Advanced Systems Outlook, in San Francisco, CA (June 5)) |

| | |
|--|-----------------|
| EXAMINER | DATE CONSIDERED |
| EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant. | |

| | | |
|--|---|------------------------------|
| PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT | ATTY. DOCKET NO. 57941.000063 | SERIAL NUMBER 10/716,596 |
| | APPLICANT(S) MICHAEL FARMWALD ET AL. | |
| | FILING DATE November 20, 2003 | GROUP ART UNIT Unassigned |

U.S. PATENT DOCUMENTS

| EXAMINER INITIALS | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|----------------------|-----|--------------------|-------------------|------------------|-------|--------------|----------------|
| | 11. | 4,330,852 | May 18, 1982 | Redwine et al. | | | |
| | 12. | 4,703,418 | Oct. 27, 1987 | James | | | |
| | 13. | 4,785,394 | Nov. 15, 1988 | Fischer | | | |
| | 14. | 4,726,021 | Feb. 16, 1988 | Horiguchi et al. | | | |
| | 15. | 4,870,562 | Sept. 26, 1989 | Kimoto et al. | | | |

FOREIGN PATENT DOCUMENTS

| EXAMINER INITIAL | | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUB CLASS | TRANSLATION YES/NO | |
|---------------------|-----|--------------------|----------------|---------|-------|--------------|-----------------------|--|
| | 16. | S56-82961 | July 7, 1981 | Japan | | | | |
| | 17. | S57-14922 | Jan. 26, 1982 | Japan | | | | |
| | 18. | Sho 60-80193 | May 8, 1983 | Japan | | | | |
| | 19. | Sho 60-55459 | Mar. 30, 1985 | Japan | | | | |
| | 20. | S61-72350 | April 14, 1986 | Japan | | | | |
| | 21. | S63-142445 | June 14, 1988 | Japan | | | | |
| | 22. | B63-46864 | Sept. 19, 1988 | Japan | | | | |
| | 23. | S64-29951 | Jan. 31, 1989 | Japan | | | | |

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

| | | |
|--|-----|---|
| | 24. | Watanabe, T.; "Session XIX: High Density SRAMS"; IEEE International Solid State Circuits Conference pp. 266-267 (1987) |
| | 25. | Ohno, C.; "Self-Timed RAM: STRAM"; Fujitsu Sci. TechJ., 24, 4, pp 293-300 (Dec. 1988) |
| | 26. | "Fast Packet Bus for Microprocessor Systems with Caches", IBM Technical Disclosure Bulletin, pp.279-282 (Jan 1989) |
| | 27. | Gustavson, D. "Scalable Coherent Interface"; Invited Paper, COMPCON Spring '89, San Francisco, CA; IEEE, pp. 536-538 (Feb 27-Mar 3, 1989) |
| | | James, D.; "Scalable I/O Architecture for Busses"; IEEE, pp. 539-544 (April 1989) |

| | |
|---|-----------------|
| EXAMINER | DATE CONSIDERED |
| EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant. | |

FEB 06 2004
PATENT & TRADEMARK OFFICE

3 of 19

| | | |
|--|---|------------------------------|
| PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT | ATTY. DOCKET NO. 57941.000063 | SERIAL NUMBER 10/716,596 |
| | APPLICANT(S) MICHAEL FARMWALD ET AL. | |
| | FILING DATE November 20, 2003 | GROUP ART UNIT Unassigned |

U.S. PATENT DOCUMENTS

| EXAMINER INITIALS | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|----------------------|-----|--------------------|-----------------|------------------|-------|--------------|----------------|
| | 28. | 4,205,373 | May 27, 1980 | Shah et al. | | | |
| | 29. | 4,845,670 | Jul. 4, 1989 | Nishimoto et al. | | | |
| | 30. | 4,509,142 | Apr. 2, 1985 | Childers | | | |
| | 31. | 4,183,095 | Jan. 8, 1980 | Ward | | | |
| | 32. | 4,685,088 | Aug. 4, 1987 | Ianucci | | | |
| | 33. | 4,975,872 | 12/04/90 | Zaiki | | | |
| | 34. | 5,016,226 | 05/14/91 | Hiwada et al. | | | |

FOREIGN PATENT DOCUMENTS

| EXAMINER INITIAL | | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUB CLASS | TRANSLATION YES/NO | |
|---------------------|-----|--------------------|----------------|---------|-------|--------------|-----------------------|--|
| | 35. | 0 246 767 | April 28, 1987 | EPO | | | | |
| | 36. | 0 334 552 | Mar. 16, 1989 | EPO | | | | |
| | 37. | 0 276 871 | Jan. 29, 1988 | EPO | | | | |

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

| | | |
|--|-----|--|
| | 38. | European Search Report for EPO Patent Application No. 00 101 1832 |
| | 39. | European Search Report for EPO Patent Application No. 89 30 2613 |
| | 40. | Z. Amitai, "New System Architectures for DRAM Control and Error Correction", Monolithic Memories Inc., Electro/87 and Mini/Mico Northeast: Focusing on the OEM Conference Record, pp. 1132, 4/31-3, (April 1987) |
| | 41. | N. Siddique, "100-MHz DRAM Controller Sparks Multiprocessor Designs", Electronic Design, pp. 138-141, (Sept 1986) |
| | 42. | H. Kuriyama et al., "A 4-Mbit CMOS SRAM WITH 8-NS SERIAL ACCESS TIME", IEEE Symposium On VLSI Circuits Digest Of Technical Papers, pp. 51-52, (June 1990) |
| | 43. | J. Chun et al., "A 1.2ns GaAs 4K Read Only Memory", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 83-86, (Nov. 1988) |
| | 44. | A. Fielder et al., "A 3 NS 1K X 4 STATIC SELF-TIMED GaAs RAM", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 67-70, (Nov. 1988) |
| | 45. | JEDEC Standard No. 21C |

| | |
|---|-----------------|
| EXAMINER | DATE CONSIDERED |
| EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant. | |

FEB 06 2004

4 of 19

| | | |
|--|---|------------------------------|
| PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT | ATTY. DOCKET NO. 57941.000063 | SERIAL NUMBER 10/716,596 |
| | APPLICANT(S) MICHAEL FARMWALD ET AL. | |
| | FILING DATE November 20, 2003 | GROUP ART UNIT Unassigned |

U.S. PATENT DOCUMENTS

| EXAMINER INITIALS | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|----------------------|-----|--------------------|------------------|--------------|-------|--------------|----------------|
| | 46. | 4,630,193 | Dec. 16, 1986 | Kris | | | |
| | 47. | 4,710,904 | Dec. 1, 1987 | Suzuki | | | |
| | 48. | 4,739,502 | Apr. 19, 1988 | Nozaki | | | |
| | 49. | 4,905,201 | Feb. 27, 1990 | Ohira et al. | | | |

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

| | |
|-----|--|
| 50. | European Search Report for EPO Patent Application No. 00 10 0018 |
| 51. | European Search Report for EPO Patent Application No. 00 10 822 |
| 52. | T.L. Jeremiah et. al., "SYNCHRONOUS PACKET SWITCHING MEMORY AND I/O CHANNEL," IBM Tech. Disc. Bul., Vol. 24, No. 10, pp. 4986-4987 (Mar. 1982) |
| 53. | L. R. Metzger, "A 16K CMOS PROM with Polysilicon Fusible Links", IEEE Journal of Solid State Circuits, vol. 18 No. 5, pp. 562-567 (Oct. 1983) |
| 54. | A. Yuen et. al., "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Feb. 1989) |
| 55. | Pelgrom et al., "A 32-kbit Variable-Length Shift Register for Digital Audio Application", IEEE Journal of Solid-State Circuits, vol. sc-22, no. 3, June 1987, pp 415-422 |
| 56. | Grover et al., "Precision Time-Transfer in Transport Networks Using Digital Crossconnect Systems", IEEE Paper 47.2 Globecom, 1988, pp 1544-1548 |
| 57. | Gustavson et al., "The Scalable Interface Project (Superbus)" (DRAFT), SCI-22 Aug 88-doc1 pp 1-16, August 22, 1988 |
| 58. | Knut Alnes, "SCI: A Proposal for SCI Operation", SCI-10Nov88-doc23, Norsk Data, Oslo, Norway, pp. 1-12, Nov. 10, 1988 |
| 59. | Knut Alnes, "SCI: A Proposal for SCI Operation", SCI-6Jan89-doc31, Norsk Data, Oslo, Norway, pp. 1-24, Jan 6, 1989 |
| 60. | Bakka et al., "SCI: Logical Level Proposals", SCI-6Jan89-doc32, Norsk Data, Oslo, Norway, pp. 1-20, Jan 6, 1989 |
| 61. | Knut Alnes, "Scalable Coherent Interface", SCI-Feb 89-doc52, (To appear in the Eurobus Conference Proceedings May 1989), pp. 1-8 |
| 62. | Boysel et al., "Four-Phase LSI Logic Offers New Approach to Computer Designer", Four-Phase Systems Inc. Cupertino, CA, Computer Design, April 1970, pp. 141-146, |
| 63. | Boysel et al., "Random Access MOS Memory Packs More Bits To The Chip", Electronics, Feb. 16, 1970, pp. 109-146, |

| | |
|--|-----------------|
| EXAMINER | DATE CONSIDERED |
| EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant. | |

| | | |
|--|---|------------------------------|
| PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT | ATTY. DOCKET NO. 57941.000063 | SERIAL NUMBER 10/716,596 |
| | APPLICANT(S) MICHAEL FARMWALD ET AL. | |
| | FILING DATE November 20, 2003 | GROUP ART UNIT Unassigned |

U.S. PATENT DOCUMENTS

| EXAMINER INITIALS | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|----------------------|-----|--------------------|----------|------------------------|-------|--------------|----------------|
| | 64. | 4,206,833 | 04/27/93 | Lee | | | |
| | 65. | 4,953,128 | 08/28/90 | Kawai et al. | | | |
| | 66. | 5,140,688 | 08/18/92 | White et al. | | | |
| | 67. | 5,018,111 | 05/21/91 | Madland | | | |
| | 68. | 4,845,664 | 07/04/89 | Aichelmann, Jr. et al. | | | |
| | 69. | 4,734,880 | 03/29/88 | Collins | | | |

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

| | |
|-----|--|
| 70. | D.T. Wong et. al., "An 11-ns 8Kx18 CMOS Static RAM with 0.5- μ m Devices", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1095-1103 (Oct. 1988) |
| 71. | T. Williams et. al., "An Experimental 1-Mbit CMOS SRAM with Configurable Organization and Operation", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1085-1094 (Oct. 1988) |
| 72. | D. Jones, "Synchronous static ram", Electronics and Wireless World, vol.93, no.1622, pp. 1243-4 (Dec. 87) |
| 73. | F. Miller et. al., "HIGH FREQUENCY SYSTEM OPERATION USING SYNCHRONOUS SRAMS", Midcon/87 Conference Record, pp. 430-432 Chicago, IL, USA; 15-17 Sept. 1987 |
| 74. | K. Ohta, "A 1-Mbit DRAM with 33-MHz Serial I/O Ports", IEEE Journal of Solid State Circuits, vol. 21 No. 5, pp. 649-654 (Oct. 1986) |
| 75. | K. Nogami et. al., "A 9-ns HIT-Delay 32-kbyte Cache Macro for High-Speed RISC", IEEE Journal of Solid State Circuits, vol. 25 No. 1, pp. 100-108 (Feb. 1990) |
| 76. | F. Towler et. al., "A 128k 6.5ns Access/ 5ns Cycle CMOS ECL Static RAM", 1989 IEEE international Solid State Circuits Conference, (Feb. 1989) |
| 77. | M. Kimoto, "A 1.4ns/64kb RAM with 85ps/3680 Logic Gate Array", 1989 IEEE Custom Integrated Circuits Conference |
| 78. | D. Wendell et. al. "A 3.5ns, 2Kx9 Self Timed SRAM", 1990 IEEE Symposium on VLSI Circuits (Feb 1990) |
| 79. | S. Watanabe et. al., "AN Experimental 16-Mbit CMOS DRAM Chip with a 100-MHz Serial READ/WRITE Mode", IEEE Journal of Solid State Circuits, vol. 24 No. 3, pp. 763-770 (June 1982) |
| 80. | K. Numata et. al. " New Nibbled-Page Architecture for High Density DRAM's", IEEE Journal of Solid State Circuits, vol. 24 No. 4, pp. 900-904 (Aug. 1989) |
| 81. | H. L. Kalter et al. "A 50-ns 16Mb DRAM with a 10-ns Data Rate and On-Chip ECC" IEEE Journal of Solid State Circuits, vol. 25 No. 5, pp. 1118-1128 (Oct 1990) |
| 82. | J. Sonntag et al. "A Monolithic CMOS 10MHz DPLL for Burst-Mode Data Retiming", IEEE International Solid State Circuits Conference (ISSCC) February 16, 1990 |

| | |
|---|-----------------|
| EXAMINER | DATE CONSIDERED |
| EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant. | |

FEB 06 2004

6 of 19

| | | |
|--|---|------------------------------|
| PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT | ATTY. DOCKET NO. 57941.000063 | SERIAL NUMBER 10/716,596 |
| | APPLICANT(S) MICHAEL FARMWALD ET AL. | |
| | FILING DATE November 20, 2003 | GROUP ART UNIT Unassigned |

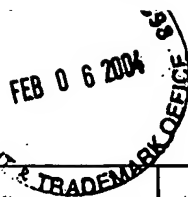
U.S. PATENT DOCUMENTS

| EXAMINER INITIALS | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|----------------------|-----|--------------------|----------|--------------------|-------|--------------|----------------|
| | 83. | 4,649,511 | 03/10/97 | Gdula | | | |
| | 84. | 4,860,198 | 08/22/89 | Takenaka | | | |
| | 85. | 3,969,706 | 07/13/76 | Proebsting et al. | | | |
| | 86. | 4,766,536 | 08/23/88 | Wilson, Jr. et al. | | | |
| | 87. | 4,998,262 | 03/05/91 | Wiggers | | | |
| | 88. | 4,757,473 | 07/12/88 | Kurihara et al. | | | |
| | 89. | 4,792,926 | 12/20/88 | Roberts | | | |
| | 90. | 4,811,202 | 03/07/89 | Schabowski | | | |
| | 91. | 5,034,917 | 07/23/91 | Bland et al. | | | |
| | 92. | 5,301,278 | 04/05/94 | Bowater et al. | | | |
| | 93. | 5,153,856 | 10/06/92 | Takahashi | | | |
| | 94. | 4,853,896 | 08/01/89 | Yamaguchi | | | |
| | 95. | 4,747,079 | 05/24/88 | Yamaguchi | | | |
| | 96. | 4,945,516 | 07/31/90 | Kashiyama | | | |
| | 97. | 4,445,204 | 04/24/84 | Nishiguchi | | | |

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

| | |
|------|--|
| 98. | M. Horowitz et. al., "MIPS-X: A 20-MIPS Peak 32-bit Microprocessor with On-Chip Cache", IEEE Journal of Solid State Circuits, vol. 22 No. 5, pp. 790-799 (Oct. 1987) |
| 99. | R. L. Schmidt, "A memory Control Chip for Formatting Data into Blocks Suitable for Video Coding Applications", IEEE Transactions on Circuits And Systems, vol. 36 No. 10, pp. 1275-1280 (Oct 1989) |
| 100. | L. R. Metzger, "A 16K CMOS PROM with Polysilicon Fusible Links", IEEE Journal of Solid State Circuits, vol. SC-18 No. 5, pp. 561-567 (Oct. 1983) |
| 101. | A. L. Yuen, "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Oct. 1989) |

| | |
|---|-----------------|
| EXAMINER | DATE CONSIDERED |
| EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant. | |



| | | |
|--|---|------------------------------|
| PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT | ATTY. DOCKET NO. 57941.000063 | SERIAL NUMBER 10/716,596 |
| | APPLICANT(S) MICHAEL FARMWALD ET AL. | |
| | FILING DATE November 20, 2003 | GROUP ART UNIT Unassigned |

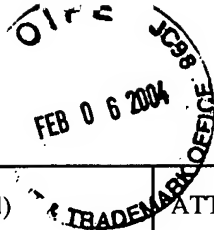
U.S. PATENT DOCUMENTS

| EXAMINER INITIALS | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|----------------------|------|--------------------|----------|----------------|-------|--------------|----------------|
| | 102. | 5,051,889 | 09/24/91 | Fung et al. | | | |
| | 103. | 5,361,277 | 11/01/94 | Grover | | | |
| | 104. | 4,954,987 | 09/04/90 | Auvinen et al. | | | |
| | 105. | 4,570,220 | 02/11/86 | Tetrick et al. | | | |
| | 106. | 4,247,817 | 01/27/81 | Heller | | | |
| | 107. | 4,519,034 | 05/21/85 | Smith et al. | | | |
| | 108. | 3,691,534 | 09/12/72 | Varadi et al. | | | |
| | 109. | 4,920,486 | 04/24/90 | Nielsen | | | |
| | 110. | 4,263,650 | 04/21/81 | Bennett et al. | | | |

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

| | | |
|--|------|--|
| | 111. | S.K. Kwon et al., "Memory Chip Organizations For Improved Reliability In Virtual Memories", IBM Technical Bulletin vol. 25 No. 6, pp. 2952-2957 (Nov 1982) |
| | 112. | J. Peterson, "System-Level Concerns Set Performance Gains", High Performance Systems, pp. 71-77 (Sept. 89) |
| | 113. | N. Margulis, "Single Chip CPU Eases Single Chip System Design", High Performance Systems, pp. 34-44 (Sept. 89) |
| | 114. | F.Nart, "Multiple Chips Speed CPU Subsystems", High Performance Systems, pp. 46-55 (Sept. 89) |
| | 115. | D.T. Wong, "An 11-ns 8Kx18 CMOS Static RAM with 0.5-um Devices", IEEE Journal of Solid State Circuits, vol. 23, No. 5, pp. 1095-1103 (Oct. 1988) |
| | 116. | A. Agarwal et al., "An Evaluation of Directory Schemes for Cache Coherence", IEEE, pp. 280-289, 1988. |

| | |
|---|-----------------|
| EXAMINER | DATE CONSIDERED |
| EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant. | |



| | | |
|--|---|------------------------------|
| PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT | ATTY. DOCKET NO. 57941.000063 | SERIAL NUMBER 10/716,596 |
| | APPLICANT(S) MICHAEL FARMWALD ET AL. | |
| | FILING DATE November 20, 2003 | GROUP ART UNIT Unassigned |

U.S. PATENT DOCUMENTS

| EXAMINER INITIALS | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|----------------------|------|--------------------|----------|--------------------|-------|--------------|----------------|
| | 117. | 4,719,602 | 01/12/88 | Hag et al. | | | |
| | 118. | 5,023,488 | 06/11/91 | Gunning | | | |
| | 119. | 4,754,433 | 06/28/88 | Chin et al. | | | |
| | 120. | 3,771,145 | 11/06/73 | Wiener | | | |
| | 121. | 5,021,985 | 06/04/91 | Hu et al. | | | |
| | 122. | 4,821,226 | 04/11/89 | Christopher et al. | | | |
| | 123. | 4,882,712 | 11/21/89 | Ohno et. al. | | | |
| | 124. | 4,951,251 | 08/21/90 | Yamaguchi et al. | | | |
| | 125. | 4,928,265 | 12/29/92 | Beighe et al. | | | |
| | 126. | 5,107,465 | 04/21/92 | Fung et al. | | | |

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

| | | |
|--|------|---|
| | 127. | D. Hawley, "Superfast Bus Supports Sophisticated Transactions", High Performance Systems, pp. 90-94 (Sept. 89) |
| | 128. | M. Bazes, A Programmable NMOS DRAM Controller for Microcomputer Systems with Dual Port Memory and Error Checking and Correction", IEEE Journal of Solid State Circuits, vol. SC-18, No. 2, pp. 164-172 (April 1983) |
| | 129. | D. Wendell et al., "A 3.5ns Self Timed SRAM", IEEE 1990 Symposium on VLSI Circuits pp. 49-50 |
| | 130. | J. Chun et al., "A pipelined 650 MHz GaAs 8K ROM with Translation Logic" IEEE 1990 GaAs IC Symposium, pp 139-142 |
| | 131. | A. L. Yuen, "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Oct. 1989) |
| | 132. | Tomoji Takada et al., "A Video Codec LSI for High-Definition TV Systems with One-Transistor DRAM Line Memories," IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, pp. 1656-1659 (Dec. 1989) |
| | 133. | Amitai, Z., "Burst Mode Memories Improve Cache Design," WESCON/90 Conference Record, pp. 29-32 (Nov. 1990) |

| | |
|---|-----------------|
| EXAMINER | DATE CONSIDERED |
| EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant. | |



| | | |
|--|---|------------------------------|
| PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT | ATTY. DOCKET NO. 57941.000063 | SERIAL NUMBER 10/716,596 |
| | APPLICANT(S) MICHAEL FARMWALD ET AL. | |
| | FILING DATE November 20, 2003 | GROUP ART UNIT Unassigned |

U.S. PATENT DOCUMENTS

| EXAMINER INITIALS | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|----------------------|------|--------------------|---------------|---------------------------|-------|--------------|----------------|
| | 134. | 4,633,735 | 05/05/87 | Novak, et. al | | | |
| | 135. | 5,684,753 | 11/04/97 | Hashimoto, et al | | | |
| | 136. | 4,322,635 | 03/30/81 | Redwine | | | |
| | 137. | 4,916,670 | 04/10/90 | Suzuki et al. | | | |
| | 138. | 5,006,982 | 04/09/91 | Ebersole et al. | | | |
| | 139. | 4,636,986 | 01/13/87 | Pinkham | | | |
| | 140. | 4,979,145 | 12/18/90 | Remington et al. | | | |
| | 141. | 5,276,846 | 01/04/94 | Aichelmann Jr., et. al | | | |
| | 142. | 4,761,567 | Aug. 2, 1988 | Walters, Jr. et al. | | | |
| | 143. | 5,101,117 | Mar. 31, 1992 | Johnson et al. | | | |

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

| | | |
|--|------|---|
| | 144. | Ikeda, Hiroaki et al., "100 MHz Serial Access Architecture for 4MB Field Memory," Symposium of VLSI Circuits, Digest of Technical Papers, pp. 11-12 (Jun. 1990) |
| | 145. | Takasugi, A. et al., "A DATA TRANSFER ARCHITECTURE FOR FAST MULTI-BIT SERIAL ACCESS MODE DRAM", 11TH European Solid State Circuits Conference, Toulouse France pp. 161-165 (Sep. 1985) |
| | 146. | Ray Pinkham et al., "A 128Kx8 70-MHz Multiport Video RAM with Auto Register Reload and 8x4 WRITE Feature," IEEE Journal of Solid State Circuits, vol. 23, no. 3, pp. 1133-1139 (Oct. 1988) |
| | 147. | Graham, Andy et al., "Pipelined static RAM endows cache memories with 1-ns speed", Electronic Design pp. 157-170 (Dec. 1984) |
| | 148. | Robert J. Lodi et al., "Chip and System Characteristics of a 2048-Bit MNOS-BORAM LSI Circuit," IEEE International Solid-State Circuits Conference, (Feb. 1976) |
| | 149. | Pinkham, Raymond, "A High Speed Dual Port Memory with Simultaneous Serial and Random Mode Access for Video Applications," IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 6, pp. 999-1007 (Dec. 1984) |
| | 150. | Ishimoto, S. et al., "A 256K Dual Port Memory," ISSCC Digest of Technical Papers, p. 38-39 (Feb. 1985) |

| | |
|--|-----------------|
| EXAMINER | DATE CONSIDERED |
| EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant. | |



| | | |
|--|---|------------------------------|
| PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT | ATTORNEY, DOCKET NO. 57941.000063 | SERIAL NUMBER 10/716,596 |
| | APPLICANT(S) MICHAEL FARMWALD ET AL. | |
| | FILING DATE November 20, 2003 | GROUP ART UNIT Unassigned |

U.S. PATENT DOCUMENTS

| EXAMINER INITIALS | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|----------------------|------|--------------------|----------|------------------|-------|--------------|----------------|
| | 151. | 4,482,999 | 11/13/84 | Janson et al. | | | |
| | 152. | 5,029,124 | 07/02/91 | Leahy et al. | | | |
| | 153. | 5,193,193 | 03/09/93 | Iyer | | | |
| | 154. | 4,926,385 | 05/15/90 | Fujishima et al. | | | |
| | 155. | 4,566,099 | 01/21/86 | Magerl | | | |
| | 156. | 4,803,621 | 02/07/89 | Kelly | | | |
| | 157. | 4,589,108 | 05/13/86 | Billy | | | |
| | 158. | 4,870,622 | 09/26/89 | Aria et al. | | | |
| | 159. | 4,878,166 | 10/31/89 | Johnson et al. | | | |
| | 160. | 4,849,965 | 07/18/89 | Chomel et al. | | | |
| | 161. | 4,851,990 | 07/25/89 | Johnson et al. | | | |

FOREIGN PATENT DOCUMENTS

| EXAMINER INITIAL | | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUB CLASS | TRANSLATION YES/NO | |
|---------------------|------|--------------------|---------------|---------|-------|--------------|-----------------------|--|
| | 162. | sho 58-31637A | Feb 24 , 1983 | Japan | | | | |
| | 163. | sho 59-165285A | Mar. 11, 1983 | Japan | | | | |
| | 164. | sho 60-261095A | June 6, 1984 | Japan | | | | |
| | 165. | sho 63-300310 | Dec. 7, 1988 | Japan | | | | |
| | 166. | hei 2-8950 | Jan 12, 1990 | Japan | | | | |
| | 167. | sho 58-184626A | Oct 28, 1983 | Japan | | | | |
| | 168. | 0 276 871 | 03/08/88 | EPO | | | | |

| | |
|---|-----------------|
| EXAMINER | DATE CONSIDERED |
| EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant. | |

| | | |
|--|---|------------------------------|
| PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT | ATTY. DOCKET NO. 57941.000063 | SERIAL NUMBER 10/716,596 |
| | APPLICANT(S) MICHAEL FARMWALD ET AL. | |
| | FILING DATE November 20, 2003 | GROUP ART UNIT Unassigned |

U.S. PATENT DOCUMENTS

| EXAMINER INITIALS | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|----------------------|------|--------------------|----------|---------------------|-------|--------------|----------------|
| | 169. | 4,528,661 | 07/09/85 | Bahr et al. | | | |
| | 170. | 4,048,673 | 09/13/77 | Hendrie et al. | | | |
| | 171. | 4,748,617 | 05/31/88 | Drewlo | | | |
| | 172. | 4,839,801 | 06/13/89 | Nicely et al. | | | |
| | 173. | 4,949,301 | 08/14/90 | Joshi et al. | | | |
| | 174. | 3,950,735 | 04/13/76 | Patel | | | |
| | 175. | 4,047,246 | 09/06/77 | Kerllenevich et al. | | | |
| | 176. | 4,763,249 | 08/09/88 | Bomba et al. | | | |
| | 177. | 4,625,307 | 11/25/86 | Tulpule et al. | | | |

FOREIGN PATENT DOCUMENTS

| EXAMINER INITIAL | | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUB CLASS | TRANSLATION YES/NO | |
|---------------------|------|--------------------|-------------------|---------|-------|--------------|-----------------------|--|
| | 178. | SHO 58-192154 | Nov. 9, 1983 | Japan | | | | |
| | 179. | SHO 63-34795 | Feb. 15, 1988 | Japan | | | | |
| | 180. | SHO 61-107453 | May 26, 1986 | Japan | | | | |
| | 181. | SHO 63-91766 | April 22, 1988 | Japan | | | | |
| | 182. | SHO 62-16289 | Jan. 24, 1987 | Japan | | | | |
| | 183. | SHO 61-160556 | Oct. 4, 1986 | Japan | | | | |

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

| | |
|------|--|
| 184. | Robert J. Lodi et al., "MNOS-BORAM Memory Characteristics," IEEE Journal of Solid-State Circuits, vol. SC-11, No. 5, pp. 622-631 (Oct. 1976) |
| 185. | Dave Bursky, "ADVANCED SELF-TIMED SRAM PARES ACCESS TIME TO 5 NS", Electronic Design, pp. 145-147 (Feb. 22, 1990) |

| | |
|---|-----------------|
| EXAMINER | DATE CONSIDERED |
| EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant. | |

FEB 06 2004

12 of 19

| | | |
|--|---|------------------------------|
| PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT | ATTY. DOCKET NO. 57941.000063 | SERIAL NUMBER 10/716,596 |
| | APPLICANT(S) MICHAEL FARMWALD ET AL. | |
| | FILING DATE November 20, 2003 | GROUP ART UNIT Unassigned |

U.S. PATENT DOCUMENTS

| EXAMINER INITIALS | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|----------------------|------|--------------------|----------|----------------|-------|--------------|----------------|
| | 186. | 3,691,534 | 09/12/72 | Veradi, et. al | | | |
| | 187. | 3,771,145 | 11/06/73 | Wiener | | | |
| | 188. | 4,536,795 | 08/20/85 | Hirota, et. al | | | |
| | 189. | 4,629,909 | 12/16/86 | Cameron | | | |
| | 190. | 4,631,659 | 12/23/86 | Hayne, et. al | | | |
| | 191. | 4,858,113 | 08/15/89 | Saccardi | | | |
| | 192. | 4,499,536 | 02/12/85 | Gemma et al. | | | |
| | 193. | 4,648,102 | 03/03/87 | Riso, et. al | | | |

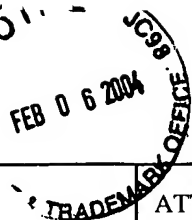
FOREIGN PATENT DOCUMENTS

| EXAMINER INITIAL | | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUB CLASS | TRANSLATION YES/NO | |
|---------------------|------|--------------------|----------|---------|-------|--------------|-----------------------|--|
| | 194. | EP 0424774 | 05/02/91 | EPO | | | | |
| | 195. | EP 0449052 | 03/29/90 | EPO | | | | |

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

| | | |
|--|------|--|
| | 196. | Hans-Jurgen Mattausch et al., "A Memory-Based High-Speed Digital Delay Line with a Large Adjustable Length," IEEE Journal of Solid-State Circuits, vol. 23, no. 1, pp. 105-110 (Feb. 1988) |
| | 197. | Lineback, J. Robert, "System Snags Shouldn't Slow the Boom in Fast Static RAMs," Electronics, pp. 60-62 (July 23, 1997) |
| | 198. | Kanopoulos, Nick and Jill H. Hallenbeck, "A First-In, First-Out Memory for Signal Processing Applications," IEEE Transactions on Circuits and Systems, Vol. CAS-33, No. 5, pp. 556-558 (May 1986) |
| | 199. | Takasugi, A. et al., "A Data-Transfer Architecture for Fast Multi-Bit Serial Access Mode DRAM," 11 th European Solid State Circuits Conference, Toulouse, France pp.161-165 (Sep. 1985) |
| | 200. | Fagan, J.L., "A 16-kbit Nonvolatile Charge Addressed Memory," IEEE Journal of Solid-State Circuits, Vol. SC-11, No. 5, pp. 631-636 (Oct. 1976) |
| | 201. | Schmitt-Landsiedel, Doris, "Pipeline Architecture for Fast CMOS Buffer RAMs," IEEE Journal of Solid-State Circuits, Vol. 25, No. 3, pp. 741-747 (Jun. 1990) |

| | |
|---|-----------------|
| EXAMINER | DATE CONSIDERED |
| EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant. | |



| | | |
|--|---|------------------------------|
| PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT | ATTY. DOCKET NO. 57941.000063 | SERIAL NUMBER 10/716,596 |
| | APPLICANT(S) MICHAEL FARMWALD ET AL. | |
| | FILING DATE November 20, 2003 | GROUP ART UNIT Unassigned |

U.S. PATENT DOCUMENTS

| EXAMINER INITIALS | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|----------------------|------|--------------------|----------------|---------------------|-------|--------------|----------------|
| | 202. | 4,825,287 | 04/25/89 | Baji, et. al | | | |
| | 203. | 4,845,677 | 07/04/89 | Chappell, et. al | | | |
| | 204. | 4,873,671 | 10/10/89 | Kowshik, et. al | | | |
| | 205. | 4,876,670 | 10/24/89 | Nakabayashi, et. al | | | |
| | 206. | 5,179,667 | 01/12/199 3 | Iyer | | | |
| | 207. | 4,901,036 | 02/13/90 | Herold, et. al | | | |
| | 208. | 4,970,418 | 11/13/90 | Masterson | | | |
| | 209. | 5,210,715 | 05/11/93 | Houston | | | |
| | 210. | 4,928,265 | 05/22/90 | Higuchi et al. | | | |
| | 211. | 4,953,130 | 08/28/90 | Houston | | | |
| | 212. | 5,251,309 | 10/05/93 | Kinoshita et al. | | | |
| | 213. | 4,099,231 | 07/01/78 | Kotok et al. | | | |

FOREIGN PATENT DOCUMENTS

| EXAMINER INITIAL | | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUB CLASS | TRANSLATION YES/NO | |
|---------------------|------|--------------------|----------|---------|-------|--------------|-----------------------|--|
| | 214. | EP 0218523 | 05/30/89 | EPO | | | | |
| | 215. | JP-A-1- 236494 | 09/21/89 | JP | | | | |
| | 216. | Sho 62-71428 | 03/27/87 | JP | | | | |
| | 217. | EP 0282735 | 09/21/88 | EPO | | | | |

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

| | | |
|--|------|--|
| | 218. | 1989 GaAs IC Data Book & Designers Guide, Gigabit Logic Inc. (Aug 1989) |
| | 219. | "IC's for Entertainment Electronics, Picture in Picture System Edition 8.89", Siemens AG, 2/89 |

| | |
|---|-----------------|
| EXAMINER | DATE CONSIDERED |
| EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant. | |

| | | |
|--|---|------------------------------|
| PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT | PATENT DOCKET NO. 57941.000063 | SERIAL NUMBER 10/716,596 |
| | APPLICANT(S) MICHAEL FARMWALD ET AL. | |
| | FILING DATE November 20, 2003 | GROUP ART UNIT Unassigned |

U.S. PATENT DOCUMENTS

| EXAMINER INITIALS | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|----------------------|------|--------------------|----------|-----------------|-------|--------------|----------------|
| | 220. | 5,099,481 | 04/24/92 | Miller | | | |
| | 221. | 5,016,226 | 05/14/91 | Hiwada, et. al | | | |
| | 222. | 5,023,835 | 06/11/91 | Akimoto, et. al | | | |
| | 223. | 5,036,495 | 07/30/91 | Busch, et. al | | | |
| | 224. | 5,111,486 | 05/05/92 | Oliboni, et. al | | | |
| | 225. | 5,123,100 | 06/16/92 | Hisada, et. al | | | |

FOREIGN PATENT DOCUMENTS

| EXAMINER INITIAL | | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUB CLASS | TRANSLATION YES/NO |
|---------------------|------|--------------------|----------|---------|-------|--------------|-----------------------|
| | 226. | WO 89/12936 | 12/28/89 | PCT | | | |
| | 227. | JP 62-51509 | 03/06/87 | Japan | | | |

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

| | | |
|--|------|--|
| | 228. | Svensson, Christer, "High Speed CMOS Chip to Chip Communications Circuit," IEEE International Symposium on Circuits and Systems, pp. 2228-2231 (Jun. 1991) |
| | 229. | Wakayama, Myles, "A 30-MHz Low-Jitter High-Linearity CMOS Voltage-Controlled Oscillator," IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 6, pp. 1074-1081 (Dec. 1987) |
| | 230. | Iqbal, Mohammad Shakaib, "Internally Timed RAMs Build Fast Writable Control Stores," Electronic Design, pp. 93-96 (August 25, 1988) |
| | 231. | Schnaitter, William M. et al., "A 0.5-GHz CMOS Digital RF Memory Chip," IEEE Journal of Solid-State Circuits, vol. SC-21, no. 5, pp. 720-726 (Oct. 1986) |
| | 232. | Whiteside, Frank, "A Dual-Port 65ns 64Kx4 DRAM with a 50MHz Serial Output," IEEE International Solid-State Circuits Conference Digest (Feb. 1986) |
| | 233. | Wu, Jich-Tsorn, "A 100-MHz Pipelined CMOS Comparator," IEEE Journal of Solid-State Circuits, Vol. 23, No. 6, pp. 1379-1385 (Dec. 1988) |
| | 234. | Motorola MC88200 Cache/Memory Management Unit User's Manual, Motorola Inc. 1989 |
| | 235. | B. Ramakrishna et al., "The Cydra 5 Departmental Supercomputer Design Philosophies, Decisions, and Trade-offs" Computer IEEE, Jan 1989 pp. 12-35 |

| | |
|---|-----------------|
| EXAMINER | DATE CONSIDERED |
| EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant. | |

| | | | |
|--|---|-----------------------------------|-----------------------------|
| PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT | PATENT & TRADEMARK OFFICE FEB 06 2004 O T P E | PATENT DOCKET NO. 57941.000063 | SERIAL NUMBER 10/716,596 |
| | APPLICANT(S) MICHAEL FARMWALD ET AL. | | |
| | FILING DATE November 20, 2003 | GROUP ART UNIT Unassigned | |

U.S. PATENT DOCUMENTS

| EXAMINER INITIALS | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|----------------------|------|--------------------|---------------|---------------|-------|--------------|----------------|
| | 236. | 4,933,953 | Jun. 12, 1990 | Yagi | | | |
| | 237. | 5,133,064 | Jul. 21, 1992 | Hotta et al | | | |
| | 238. | 5,184,027 | Feb. 2, 1993 | Masuda et al. | | | |

FOREIGN PATENT DOCUMENTS

| EXAMINER INITIAL | | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUB CLASS | TRANSLATION YES/NO |
|---------------------|------|--------------------|---------------|---------|-------|--------------|-----------------------|
| | 239. | JP 1284132 | Nov 15, 1989 | Japan | | | |
| | 240. | EP 0 329 418 A2 | Aug 23, 1989 | EPO | | | |
| | 241. | JP 1043894 | Feb. 16, 1989 | Japan | | | |

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

| | | |
|--|------|--|
| | 242. | "Intel MCS-4 Micro Computer Set", Intel Corporation, Santa Clara, CA, 1972, (pp.1-12) |
| | 243. | "MIPS R3010 coprocessor", IEEE Micro June 1988, (pp.54-62) |
| | 244. | "Intel MCS-4 Micro Computer Set Users Manual", Intel Corporation, Santa Clara, CA, March 1972, (pp.1-26, and 60-68) |
| | 245. | "Bipolar/MOS Memories Data Book", Advanced Micro Devices, Sunnyvale, CA, 1986 (pp. 4-143 to 4-163) |
| | 246. | "Memories 1986-87 Databook", Fujitsu Inc., 1986 (pp. 1-102 to 1-128) |
| | 247. | "MIPS Chip Set Implements Full ECL CPU" Microprocessor Report, MicroDesign Resources Inc., Vol. 3: No. 12; Dec. 1989 |
| | 248. | "R6000 System Bus & R6020 SBC Specification" MIPS Computer Systems Inc., Sunnyvale, CA, Aug 22, 1989 |
| | 249. | R.A. Volz et al., "POSITION PAPER ON GLOBAL CLOCK FOR THE FUTUREBUS +", SCI - 1989 - doc-59, pp. 1-9 |
| | 250. | "ECL bus controller hits 266 Mbytes/s" Microprocessor Report, MicroDesign Resources Inc., Vol. 4: No. 1; Pg. 12, Jan. 24, 1990 |

| | |
|---|-----------------|
| EXAMINER | DATE CONSIDERED |
| EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant. | |

| | | | |
|--|--|-----------------------------------|-----------------------------|
| PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT | PATENT & TRADEMARK OFFICE FEB 06 2004 | PATENT DOCKET NO. 57941.000063 | SERIAL NUMBER 10/716,596 |
| | APPLICANT(S) MICHAEL FARMWALD ET AL. | | |
| | FILING DATE November 20, 2003 | GROUP ART UNIT Unassigned | |

U.S. PATENT DOCUMENTS

| EXAMINER INITIALS | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|----------------------|------|--------------------|------------------|-------------------|-------|--------------|----------------|
| | 251. | 4,922,141 | May 1, 1990 | Lofgren et al. | | | |
| | 252. | 4,253,147 | Feb. 24, 1981 | MacDougall et al. | | | |
| | 253. | 4,975,877 | Dec. 4, 1990 | Bell | | | |
| | 254. | 4,712,194 | Dec. 8, 1987 | Yamaguchi | | | |
| | 255. | 5,287,532 | Feb. 15, 1994 | Hunt | | | |
| | 256. | 5,157,776 | Oct. 20, 1992 | Foster | | | |
| | 257. | 5,023,838 | Jun. 11, 1991 | Herbert | | | |
| | 258. | 4,961,171 | Oct. 2, 1990 | Pinkham et al. | | | |

FOREIGN PATENT DOCUMENTS

| EXAMINER INITIAL | | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUB CLASS | TRANSLATION YES/NO |
|---------------------|------|--------------------|------------------|-------------------|-------|--------------|-----------------------|
| | 259. | 0 329 418 | Aug. 23, 1989 | United Kingdom | | | |

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

| | | |
|--|------|---|
| | 260. | Ralston, E.D. Reilly, "Encyclopedia of Computer Science", Chapman & Hall, 1983, page 1471 |
| | 261. | S.A. Ward, R.H. Halstead, "Computation Structures", The MIT Press, McGraw-Hill Book Company, 1990, pages, 174-175, 93, 250-251, and 258-259 |
| | 262. | Betty Prince, "Semiconductor Memories", Second Edition, John Wiley & Sons, 1991, pages 251, 310, 314, 200-201, 467 |

| | |
|---|-----------------|
| EXAMINER | DATE CONSIDERED |
| EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant. | |

OIP
FEB 06 2004
PATENT & TRADEMARK OFFICE

| | | |
|--|---|------------------------------|
| PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT | PATENT NO. 57941.000063 | SERIAL NUMBER 10/716,596 |
| | APPLICANT(S) MICHAEL FARMWALD ET AL. | |
| | FILING DATE November 20, 2003 | GROUP ART UNIT Unassigned |

U.S. PATENT DOCUMENTS

| EXAMINER INITIALS | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|----------------------|------|--------------------|---------------|-----------------|-------|--------------|-------------|
| | 263. | 4,930,065 | May 22, 1990 | McLagan et al. | | | |
| | 264. | 4,782,439 | Nov. 1, 1988 | Borkar et al. | | | |
| | 265. | 4,747,081 | May 24, 1988 | Heilveil et al. | | | |
| | 266. | 4,704,678 | Nov. 3, 1987 | May | | | |
| | 267. | 4,644,469 | Feb. 17, 1987 | Sumi | | | |
| | 268. | 4,641,276 | Feb. 3, 1987 | Dunki-Jacobs | | | |
| | 269. | 4,639,890 | Jan. 27, 1987 | Heilveil et al. | | | |
| | 270. | 4,468,733 | Aug. 28, 1984 | Oka et al. | | | |
| | 271. | 4,426,685 | Jan. 17, 1984 | Lorentzen | | | |
| | 272. | 4,408,272 | Oct. 4, 1983 | Walters | | | |
| | 273. | 4,257,097 | Mar. 17, 1981 | Moran | | | |
| | 274. | 3,846,763 | Nov. 5, 1974 | Riikonen | | | |
| | 275. | H696 | Oct. 3, 1989 | Davidson | | | |

FOREIGN PATENT DOCUMENTS

| EXAMINER INITIAL | | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUB CLASS | TRANSLATION YES/NO | |
|---------------------|------|--------------------|---------------|---------|-------|--------------|-----------------------|--|
| | 276. | 61028248 | Feb. 7, 1986 | Japan | | | | |
| | 277. | 58184647 | Oct. 28, 1983 | Japan | | | | |

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

| | |
|------|--|
| 278. | Hopper et al., <i>Multiple vs. Wide Shared Bus Multiprocessors</i> , Proceedings of the 16 th Annual International Symposium on Computer Architecture, Jerusalem, Israel, June 1989, IEEE Computer Society Press, 1989. |
| 279. | Gehring et al., <i>A Survey of Commercial Parallel Processors</i> , Computer Architecture News, Vol. 16, No. 4, Sept. 1988. |
| 280. | Dubois et al. <i>Effects of Cache Coherency in Multiprocessors</i> , IEEE Transaction in Computers, Vol. C31, No. 11, pgs. 1083-1099, November 1982. |

| | |
|---|-----------------|
| EXAMINER | DATE CONSIDERED |
| EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant. | |



| | | |
|--|---|------------------------------|
| PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT | ATTY. DOCKET NO. 57941.000063 | SERIAL NUMBER 10/716,596 |
| | APPLICANT(S) MICHAEL FARMWALD ET AL. | |
| | FILING DATE November 20, 2003 | GROUP ART UNIT Unassigned |

U.S. PATENT DOCUMENTS

| EXAMINER INITIALS | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|----------------------|------|--------------------|---------------|---------------|-------|--------------|----------------|
| | 281. | 5,847,997 | Dec. 8, 1998 | Harada et al. | | | |
| | 282. | 5,148,523 | Sep 15, 1992 | Harlin et al. | | | |
| | 283. | 5,142,637 | Aug. 25, 1992 | Harlin et al. | | | |
| | 284. | 5,109,498 | Apr. 28, 1992 | Kamiya et al. | | | |

FOREIGN PATENT DOCUMENTS

| EXAMINER INITIAL | | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUB CLASS | TRANSLATION YES/NO |
|---------------------|------|--------------------|---------------|---------|-------|--------------|-----------------------|
| | 285. | 120553/1987 | Jun. 1, 1987 | Japan | | | |
| | 286. | 0 189 576 | Aug. 6, 1986 | EPO | | | |
| | 287. | 0 187 289 | Jul. 16, 1986 | EPO | | | |
| | 288. | 0 166 192 | Jan. 2, 1986 | EPO | | | |
| | 289. | 0 126 976 | Dec. 5, 1984 | EPO | | | |
| | 290. | 135684/1984 | Aug. 3, 1984 | Japan | | | |
| | 291. | 82/02615 | Aug. 5, 1982 | PCT | | | |

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

| | | |
|--|------|--|
| | 292. | S. Muchmore, <i>Designing Computer Systems Based on Multibus II</i> , New Electronics, Vol. 20, No. 16, p. 31-32, Aug. 11, 1987. |
| | 293. | T.C. Poon et al., <i>A CMOS DRAM-Controller Chip Implementation</i> , IEEE Journal of Solid State Circuits, Vol. 22, No. 3, pp. 491-494, Jun. 1987. |
| | 294. | <i>Accordion Start-Stop Sequencer for a Variable Cycle Storage Controller</i> , IBM Technical Disclosure Bulletin, pp. 2074-2075, (a delphion.com reprint on two sheets), Oct. 1986. |
| | 295. | <i>Motorola 68030 Cache Organization</i> , posting to Internet Newsgroup net.arch by aglew@ccvaxa.UUCP , (a google.com reprint on two sheets), Sep. 29, 1986. |
| | 296. | Stanley D. Rosenbaum et al., <i>A 16 384-Bit High-Density CCD Memory</i> , IEEE Journal of Solid State Circuits, Vol. SC-11, No. 1, pp. 33-39, Feb. 1976 |

| | |
|---|-----------------|
| EXAMINER | DATE CONSIDERED |
| EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant. | |



| | | |
|--|---|------------------------------|
| PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT | PATENT DOCKET NO. 57941.000063 | SERIAL NUMBER 10/716,596 |
| | APPLICANT(S) MICHAEL FARMWALD ET AL. | |
| | FILING DATE November 20, 2003 | GROUP ART UNIT Unassigned |

U.S. PATENT DOCUMENTS

| EXAMINER INITIALS | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|----------------------|------|--------------------|---------------|--------------------|-------|--------------|----------------|
| | 297. | 5,083,296 | Jan. 21, 1992 | Hara et al. | | | |
| | 298. | 5,077,693 | Dec. 31, 1991 | Hardee et al. | | | |
| | 299. | 4,937,734 | Jun. 26, 1990 | Bechtolsheim | | | |
| | 300. | 4,920,483 | Apr. 24, 1990 | Pogue et al. | | | |
| | 301. | 4,912,630 | Mar. 27, 1990 | Cochcroft, Jr. | | | |
| | 302. | 4,807,189 | Feb. 21, 1989 | Pinkham et al. | | | |
| | 303. | 4,799,199 | Jan. 17, 1989 | Scales, III et al. | | | |
| | 304. | 4,788,667 | Nov. 29, 1988 | Nakano et al. | | | |
| | 305. | 4,680,738 | Jul. 14, 1987 | Tam | | | |
| | 306. | 4,675,850 | Jun. 23, 1987 | Kumanoya et al. | | | |
| | 307. | 4,315,308 | Feb. 9, 1982 | Jackson | | | |
| | 308. | 4,092,665 | May 30, 1978 | Saran | | | |
| | 309. | 4,084,154 | Apr 11, 1978 | Panigrahi | | | |
| | 310. | 3,821,715 | Jun. 28, 1974 | Hoff, Jr. et al. | | | |
| | 311. | 4,016,545 | Apr. 5, 1977 | Lipovski | | | |

| | |
|---|-----------------|
| EXAMINER | DATE CONSIDERED |
| EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant. | |